Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1, 2, 4 - 12 and 14 - 20 are presently pending in the application. Claims 1 - 4 and 14 - 19 are subject to examination and claims 5 - 12 and 20 have been withdrawn from examination. Claim 1 has been amended. Claim 3 has been canceled.

On page 2 of the above-identified Office Action, claims 1, 2 and 14 - 19 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,323,509 to Kusunoki ("**KUSUNOKI**") in view of U. S. Patent Application Publication No. 2001/0040255 to Tanaka ("**TANAKA**"). On page 5 of the Office Action, claims 1 - 4 and 15 - 19 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 4,689,647 to Nakagawa ("**NAKAGAWA**") in view of U. S. Patent Application Publication No. 2001/0040255 to Tanaka ("**TANAKA**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

More particularly, Applicants' amended claim 1 recites, among other limitations:

> a semiconductor substrate forming an inner zone and having a front side, a rear side, and a **peripheral annular high-voltage edge;**
>
> said front side of said semiconductor substrate having semiconductor wells of a first conductivity type formed therein with transistor cells within said peripheral annular high-voltage edge, **said peripheral annular high-voltage edge being provided on said front side of said semiconductor substrate;** [emphasis added by Applicants]

As such, Applicants' invention requires, among other limitations, a high-voltage edge on the main surface on the front side of the semiconductor substrate. This is supported in paragraph [0038] of the instant application, which states, in part:

> The active region of the IGBT is covered with a metal layer 38a and surrounded on the outside **by an annular high-voltage edge 31** toward the chip edge. [emphasis added by Applicants]

Figs. 3A and 3B of the instant application, showing the annular high-voltage edge 31, is reproduced below, for convenience.

FIG 3A

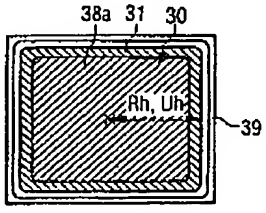
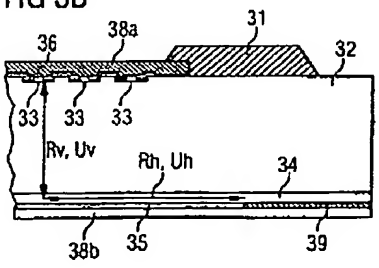


FIG 3B



Additionally, Applicants' claim 1 has been amended to include the limitation of former claim 3. Applicants' amended claim 1 recites, among other limitations,

> at least one emitter region of the first conductivity type formed at said rear side of said semiconductor substrate;
>
> **at least one emitter short region** of a second conductivity type **integrated substantially only in a region of said high-voltage edge**, said at least one emitter short region lying in a plane with said at least one emitter region and forming an electrode of the antiparallel diode, **said at least one emitter short region extending as far as a chip end in edge regions of the IGBT**;
>
> **said at least one emitter region having no emitter short regions within said high-voltage edge**; [emphasis added by Applicants]

The above limitations of amended claim 1 are additionally supported by the specification of the instant application, as well as the originally filed claims. More particularly, paragraph [0038] of the instant application further states, in part:

> A p-conducting emitter region 35 is arranged on the rear side of the IGBT. The p-conducting emitter region 35 is extended right into the region below the high-voltage edge 31. **An electrode of the monolithic integrated antiparallel diode is formed in the form of an n-conducting emitter short region 39, which preferably adjoins the emitter region 35 as far as toward the outer edge of the device. This emitter short region 39 extends only in the region of the high-voltage edge 31, and the emitter regions 35 have no emitter shorts, as is shown in FIG. 3B.** [emphasis added by Applicants]

The above features of Applicants' claims, among others, are not shown in the cited references.

As stated above, Applicants' amended claim 1 recites, among other limitations, that the high voltage edge is provided on the main surface in the form of an annular ring. page 2 of the Office Action analogizes Applicants' formerly claimed "peripheral high-voltage edge" to the "region where p-regions 28 are located" in **KUSONOKI**. However, **KUSUNOKI** neither teaches, nor suggests **a peripheral annular high-voltage edge"** provided on the front side of the semiconductor substrate, as recited in Applicants' claim 1. **KUSUNOKI** doesn't provide more than p-doped regions 28 around the cell region.

Further, the **NAKAGAWA** reference additionally fails to teach or suggest, among other limitations of Applicants' amended claim **1, at least one emitter short region integrated substantially only in a region of the high-voltage edge, the at least one emitter short region extending as far as a chip end in edge regions of the IGBT.** Rather, although **NAKAGAWA** discloses an emitter-short 21 lying in the region opposite a high-voltage edge, **the emitter short does not extend to the chip end.** In the embodiment shown in Fig. 6 of **NAKAGAWA**, an emitter short is shown at the chip edge, **however, there does not appear to**

be a high-voltage edge. Thus, NAKAGAWA neither teaches, nor suggests, all limitations of Applicant's claim 1.

The **TANAKA** reference, cited in the Office Action in combination with **KUSONOKI** and **NAKAGAWA** does not teach or suggest the above limitations missing from **KUSONOKI** and **NAKAGAWA**. As such, the **KUSONOKI** and **NAKAGAWA**, taken alone, or in combination with **TANAKA**, fail to teach or suggest all limitations of Applicants' claim 1.

Additionally, Applicant notes that on pages 3 and 5 - 6 of the Office, it is stated, in part:

> Note that the limitation "doping with a dose of between $1x10^{12}$ and $1x10^{15}$ charge carriers per cm^3" is merely a product-by process limitation. The specified does (which is a process step) does not necessarily impart a specific dopant concentration. Therefore, the product-by-process limitation does not structurally/patentably [sic] the claimed product over the prior art.

Applicants respectfully disagree. Applicants' claim 1 outlines the **thickness**, as well as, **the dose** for the doping material in the emitter region. Since the **doping concentration can be determined from the thickness and the dose**, Applicants' specific doping concentration is specified by claim 1, which recites, among other limitations:

> said at least one emitter region **having a thickness of less than 1 micrometer** and a doping with a dose of

between $1 \cdot 10^{12}$ and $1 \cdot 10^{15}$ charge carriers per cm^2;
[emphasis added by Applicants]

And thus, the above is not merely a product-by-process limitation, and needs to be given patentable weight in the claim.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1, 2, 4 - 12, and 13 - 20 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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For Applicants

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